Device Processing Development for Resonant Enhanced Modulators

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August 1,2001

Outline of the Presentation

I.) Summary of Work

II.) Processing Technology Development

- A.) InP/InGaAsP etching
- B.) Electron-Beam Lithography
- C.) Mask Transfer

III.) Transfer to the JEOL E-beam

IV.) Future Plans

V.) Conclusions

Acknowledgements

From the University of Illinois at Urbana Champaign, we would like to thank John S. Hughes, Wu Lu, and Gabriel Cueva for their assistance and technical support related to the electron beam lithography; we would also like to thank Ling Zhou of the University of Illinois for providing Auger measurements.

July-September 2000:

- Project Initiated
- Developed a Cl_2-based anisotropic ICP-RIE process to etch InP

October 2000-March 2001:

- Developed an e-beam lithography process on the Leica 10.5 EBMF ebeam to realize ring resonators
- Optimized etching for heterostructures with InGaAsP
- Delivered Sarnoff with initial device samples

April 2001-May 2001:

- Refined hard etch mask proces
- Began routine deliveries to Sarnoff (late April)

June 2001-present:

- Began process development on the JEOL 6000FS ebeam; demonstrated superior devices

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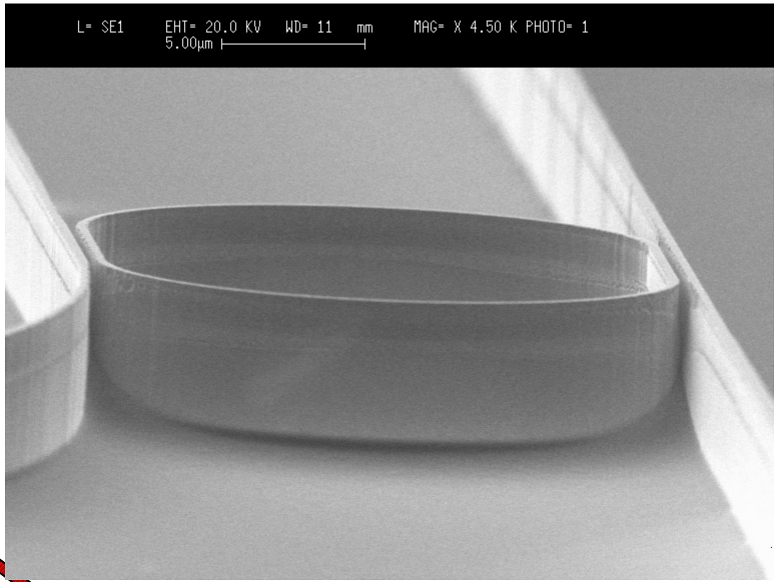
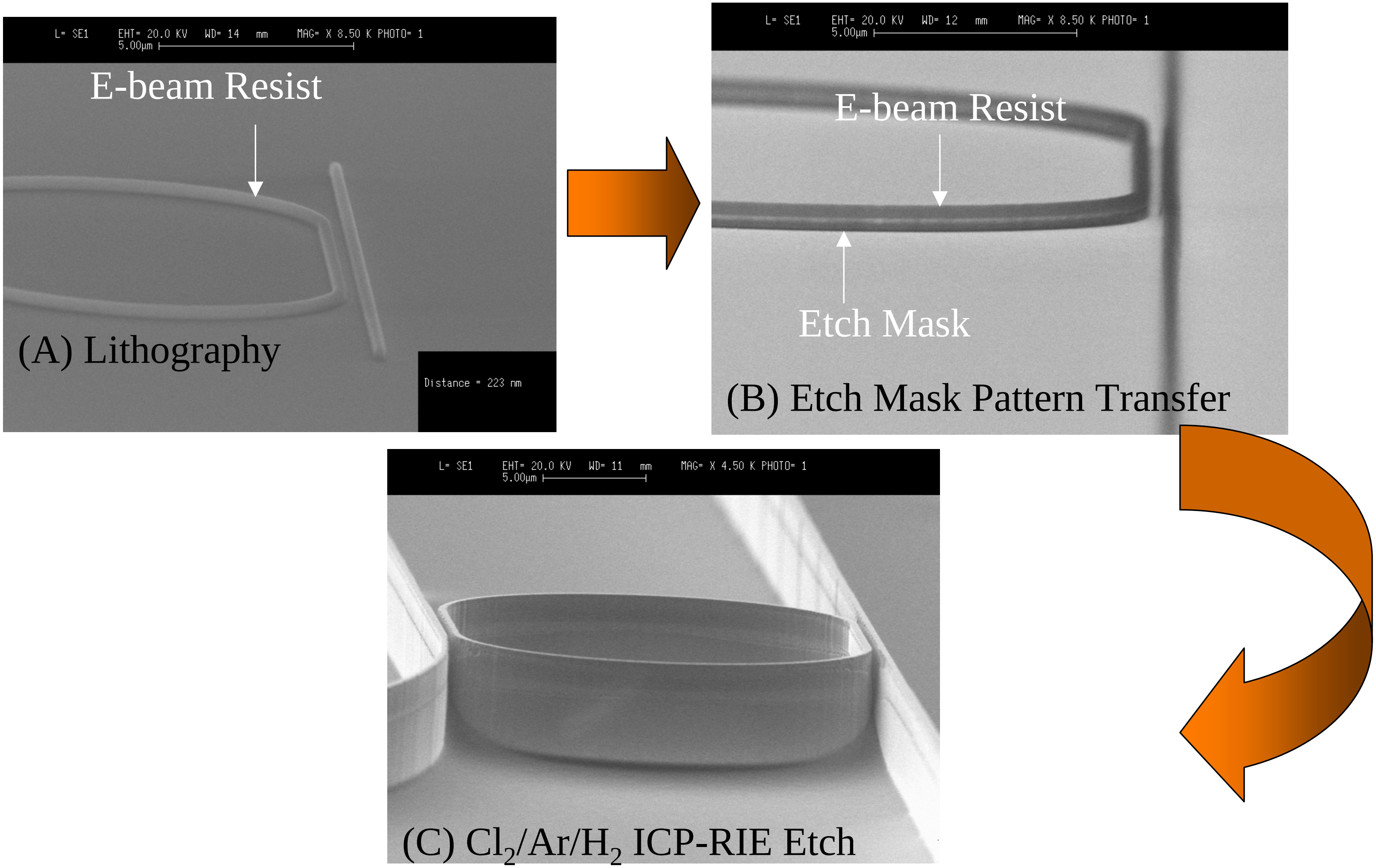
Critical Processing Processing Technologies



Electron-Beam Lithography

Masking Material/ Pattern Transfer

InP Etching


L= SE1 EHT= 20.0 KV WD= 14 mm MAG= X 8.50 K PHOTO= 1
5.00µm
E-beam Resist
(A) Lithography
Distance = 223 nm
L= SE1 EHT= 20.0 KV WD= 12 mm MAG= X 8.50 K PHOTO= 1
5.00µm
E-beam Resist
Etch Mask
(B) Etch Mask Pattern Transfer
L= SE1 EHT= 20.0 KV WD= 11 mm MAG= X 4.50 K PHOTO= 1
5.00µm
(C) $Cl_2/Ar/H_2$ ICP-RIE Etch

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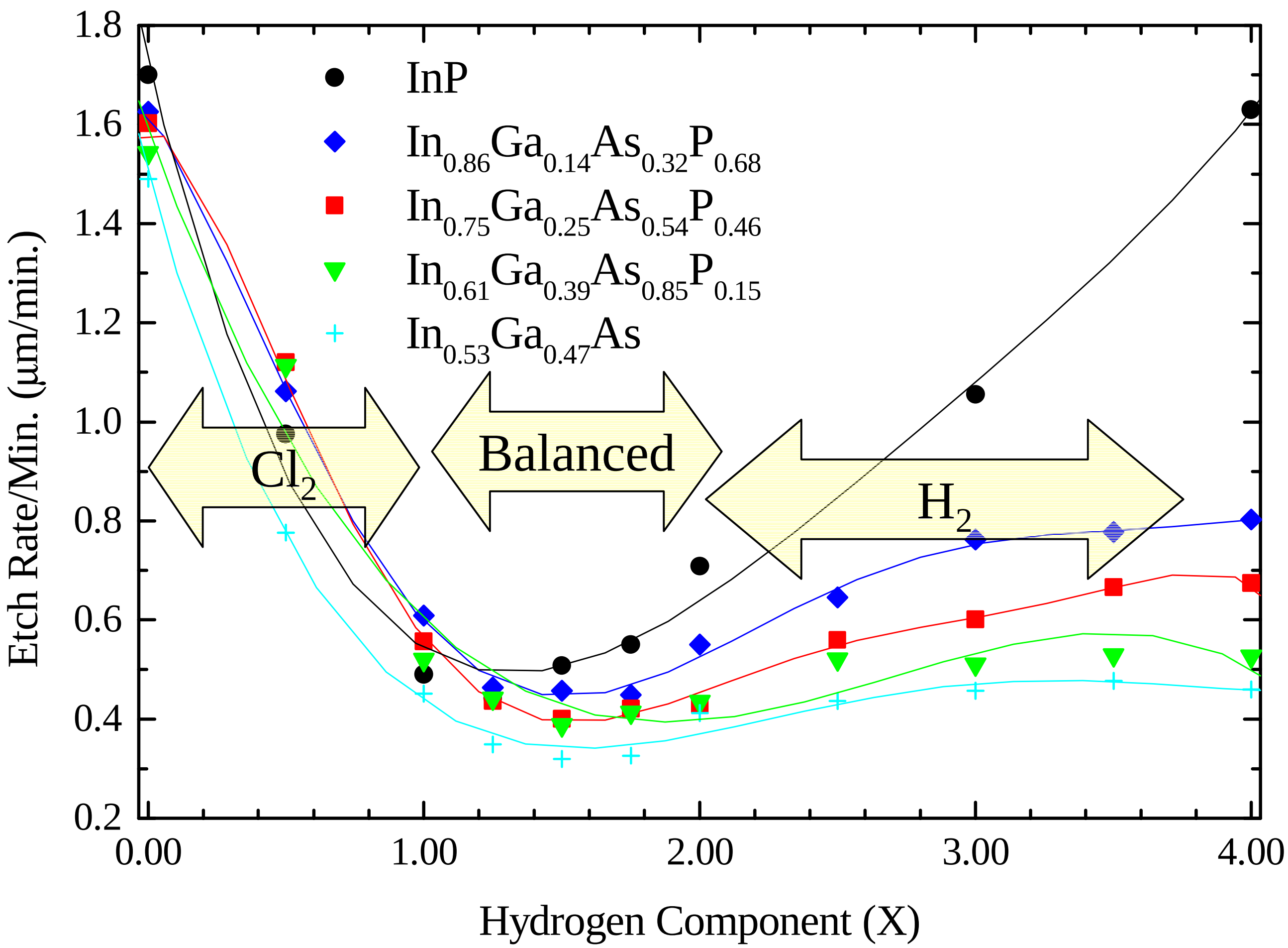
2 Cl_2/ 3 Ar/ X H_2 Etch of InP, InGaAs, and InGaAsP



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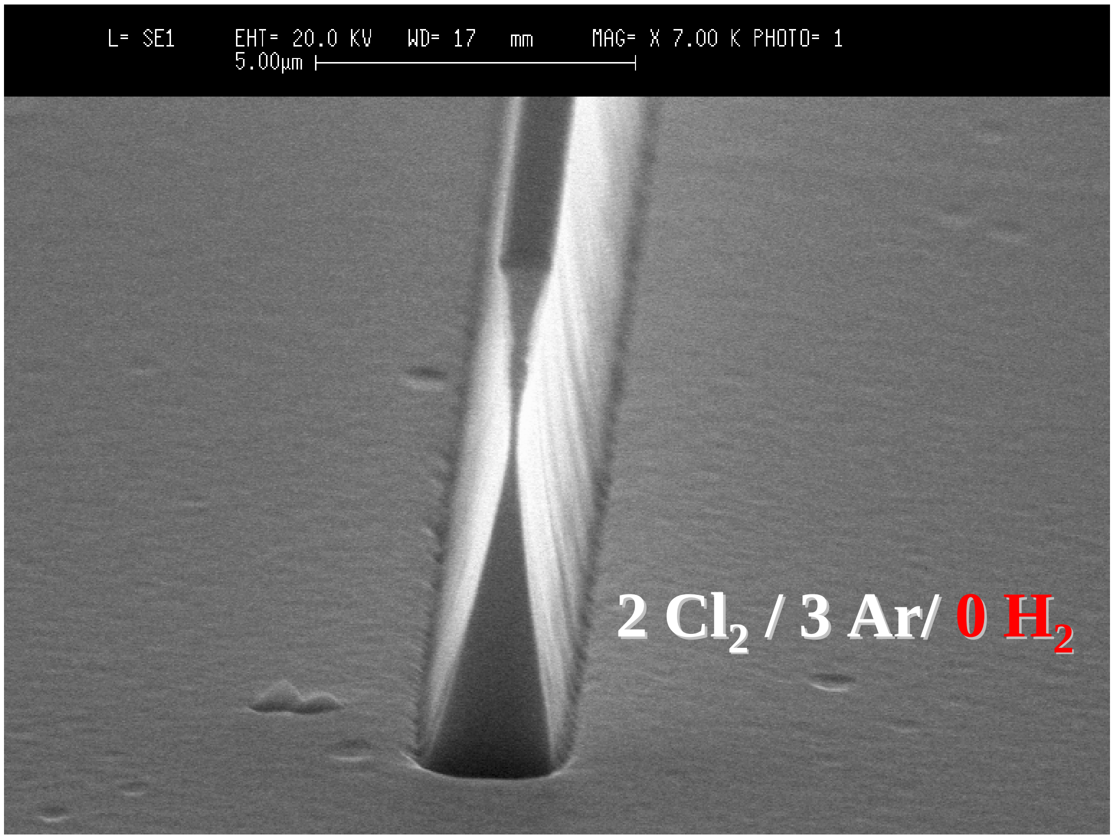
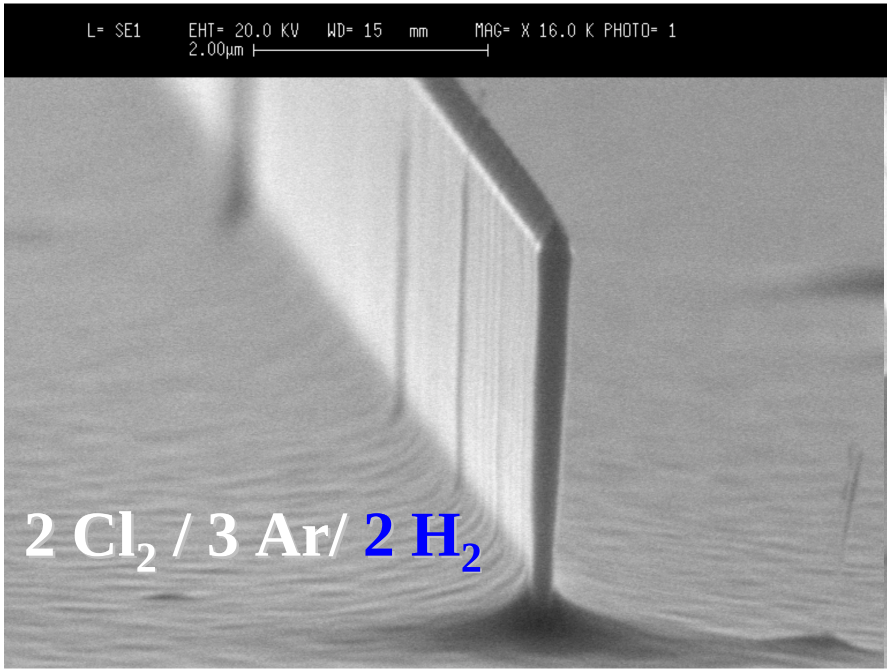
Cl_2 - Dominated Regime:

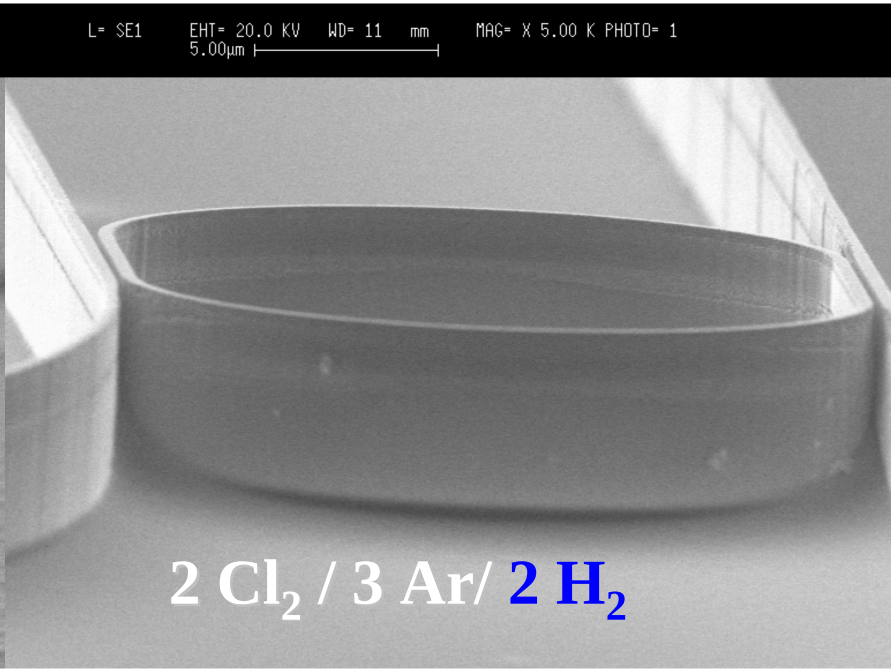
High Undercut of InP



51 nm	$In_{0.53}Ga_{0.47}As$
1410 nm	InP
300 nm	$In_{0.86}Ga_{0.14}As_{0.32}P_{0.68}$
100 nm	$In_{0.75}Ga_{0.25}As_{0.54}P_{0.46}$
300 nm	$In_{0.86}Ga_{0.14}As_{0.32}P_{0.68}$
1500 nm	InP
InP Substrate	

Minimum Etch Rate (Balanced) Regime: *High Anisotropy Achieved*





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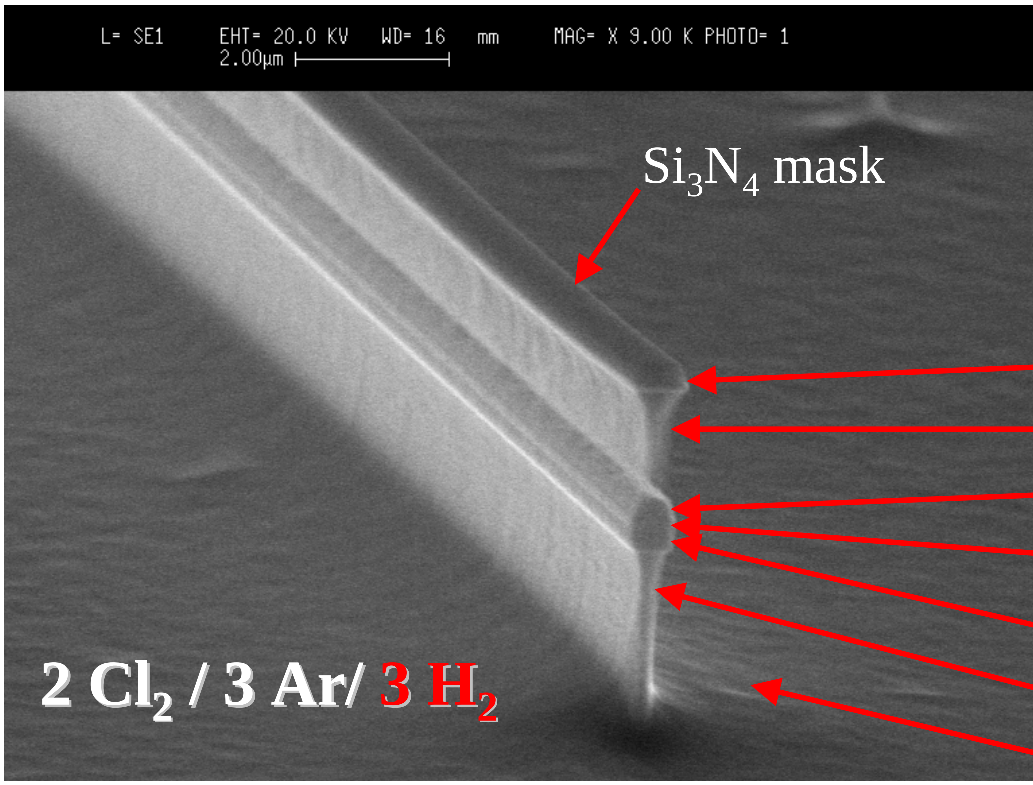
300 nm	$In_{0.86}Ga_{0.14}As_{0.32}P_{0.68}$
1500 nm	InP
InP Substrate	

H_2 - Dominated Regime:
High Undercut of InP; Selective Etching of InP Compared to InGaAsP



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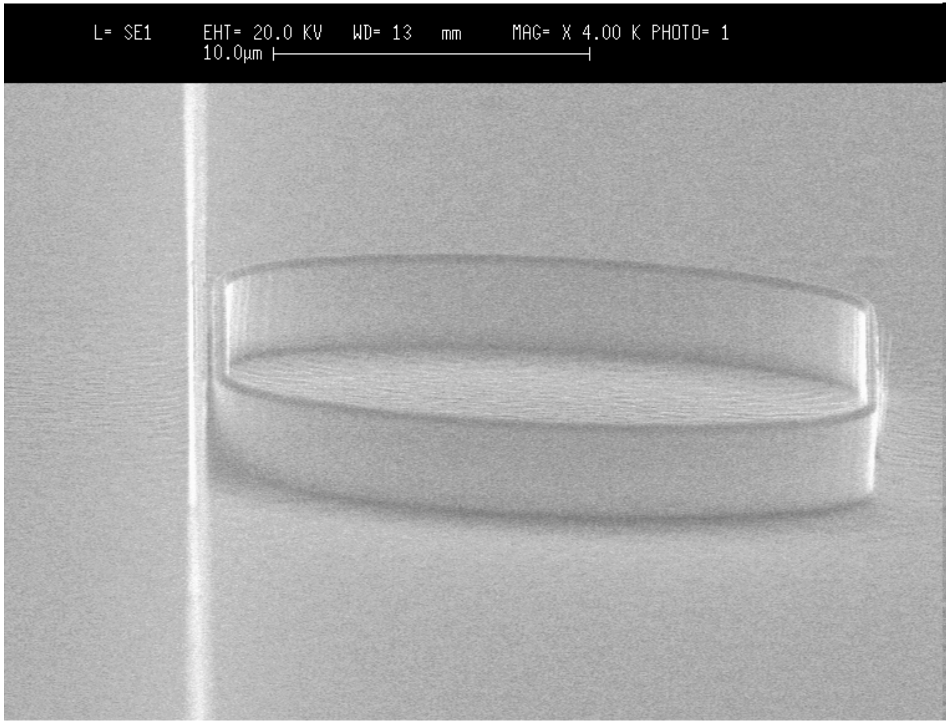
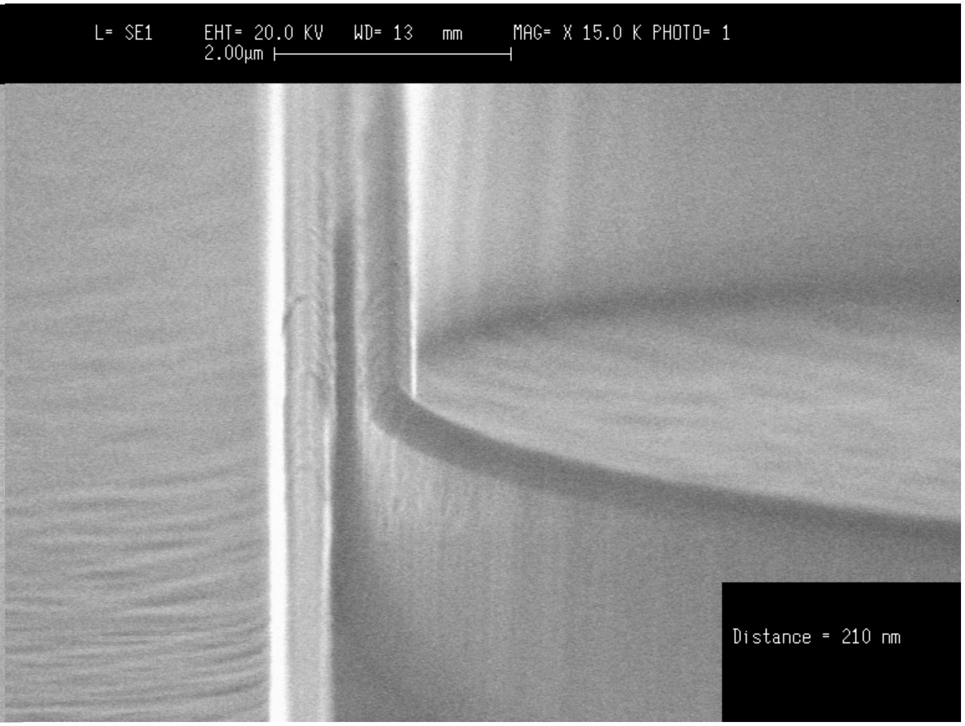
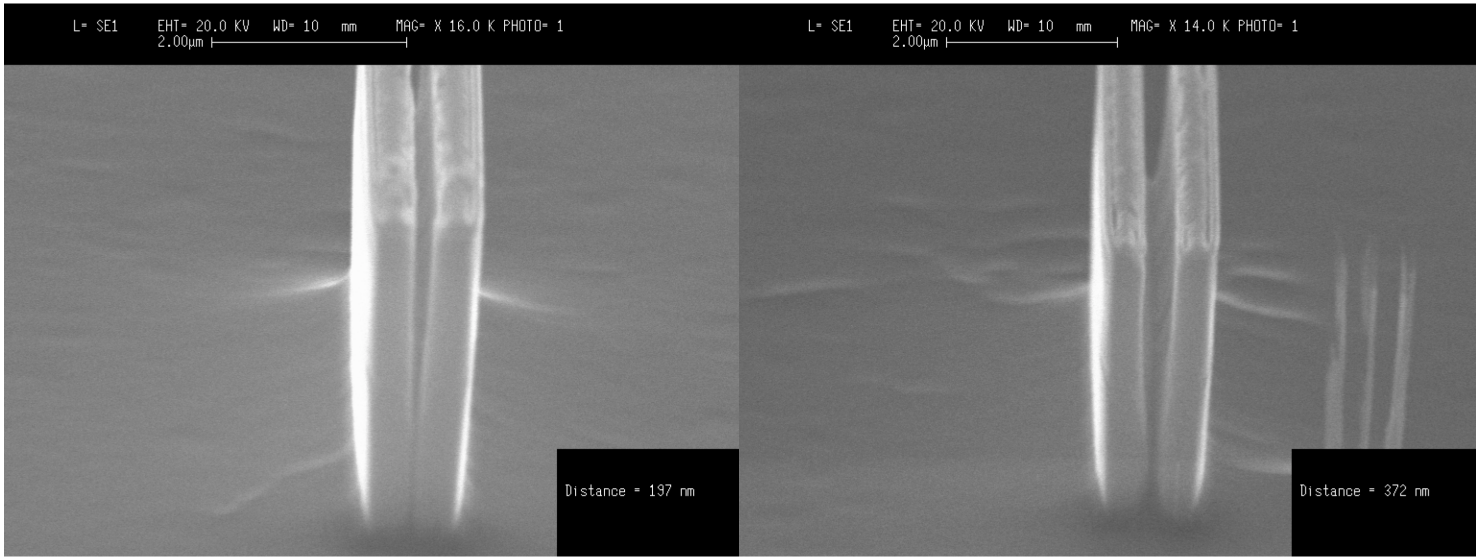
InP Substrate	


L= SE1 EHT= 20.0 KV WD= 13 mm MAG= X 4.00 K PHOTO= 1
10.0µm

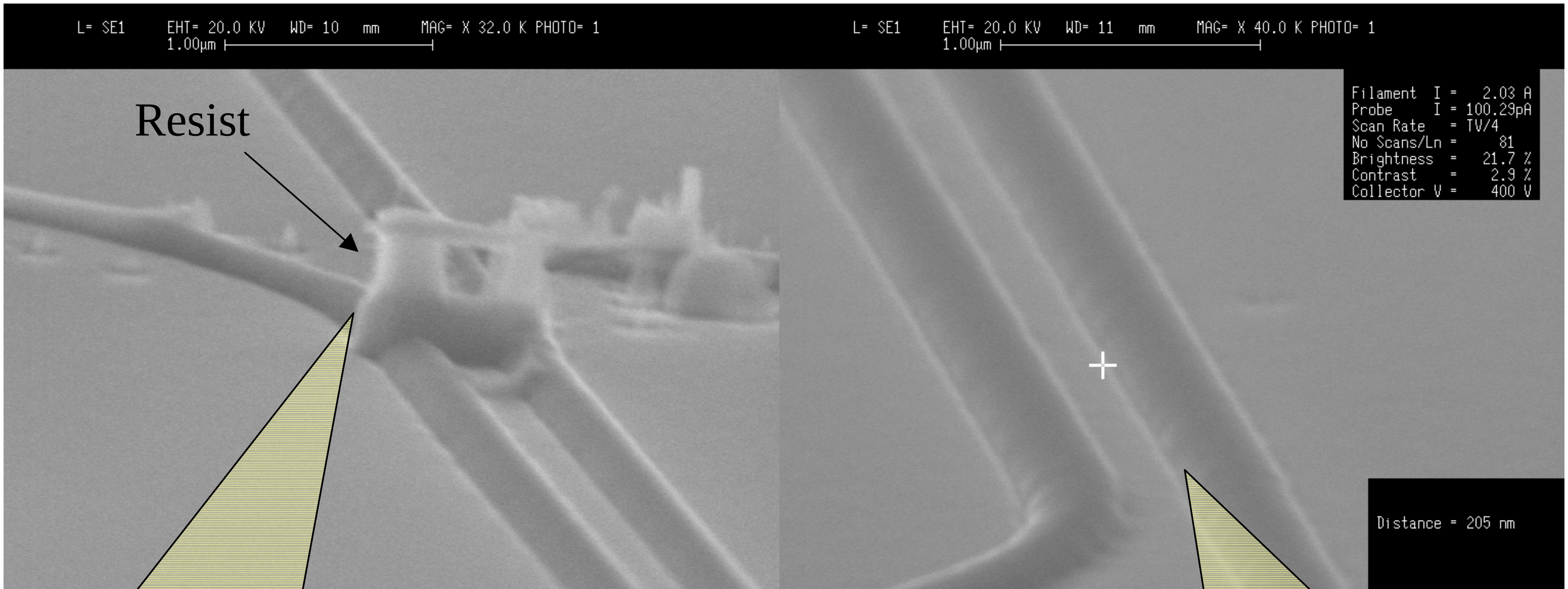

L= SE1 EHT= 20.0 KV WD= 13 mm MAG= X 15.0 K PHOTO= 1
2.00µm
Distance = 210 nm

Aspect Ratio Dependence of the Etch: Isolation in the Gap



- Etching in the small gaps proceeds at a slower rate than the bulk regions..
- When the bulk is etched 3 µm, the gap is only etched 2 µm
- To ensure isolation, we must etch the sample deeper!
- Seems simple, but……….

Using SF_6 to etch thick Si_3N_4 masks (>350 nm) resulted in undesirable etch mask profiles:



Original thickness (protected by a flake of dust).

Mask has a curved profile => fast erosion

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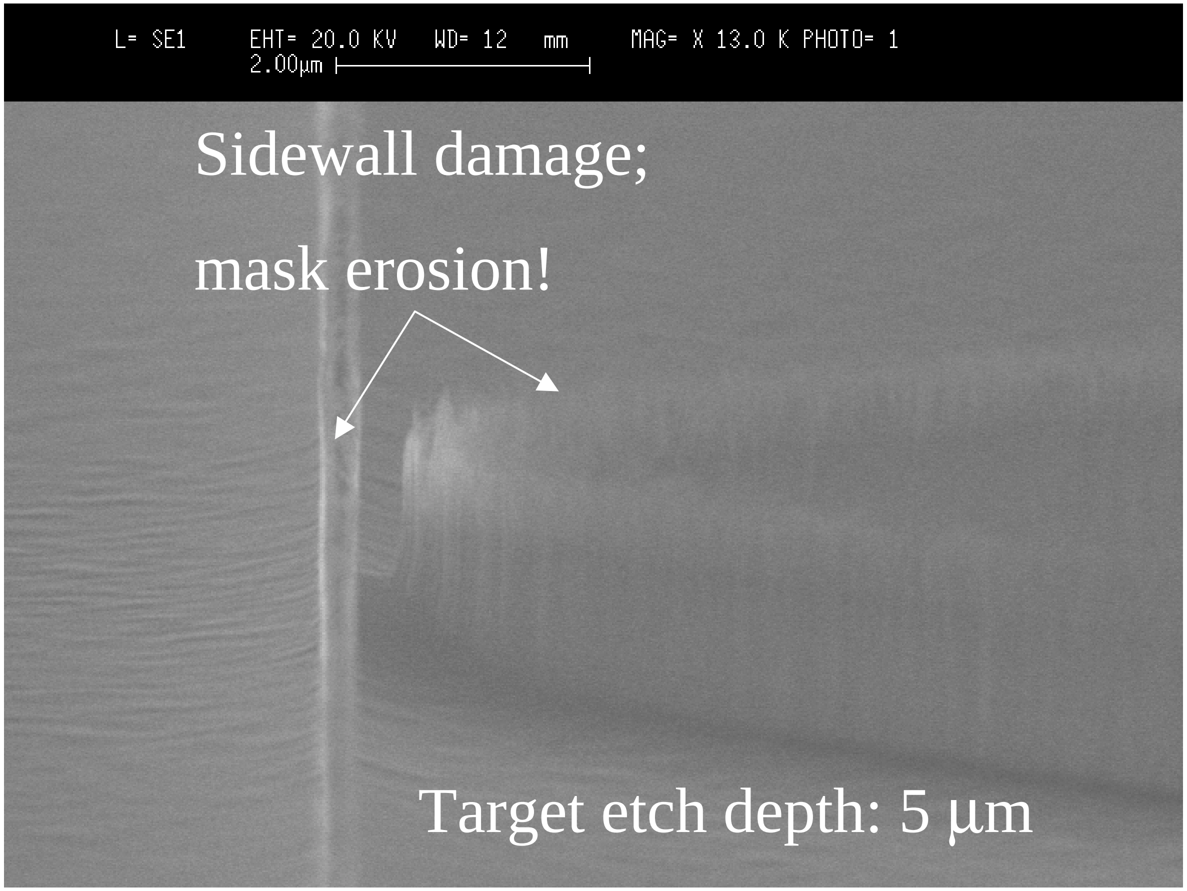
Key Problems with SF_6-patterned Si_3N_4 etch masks:

Mask Erosion Limited Sample Etch Depth to ~3.5 µm:

Insufficient for Isolation! **Rough Sidewalls=> High Loss!**



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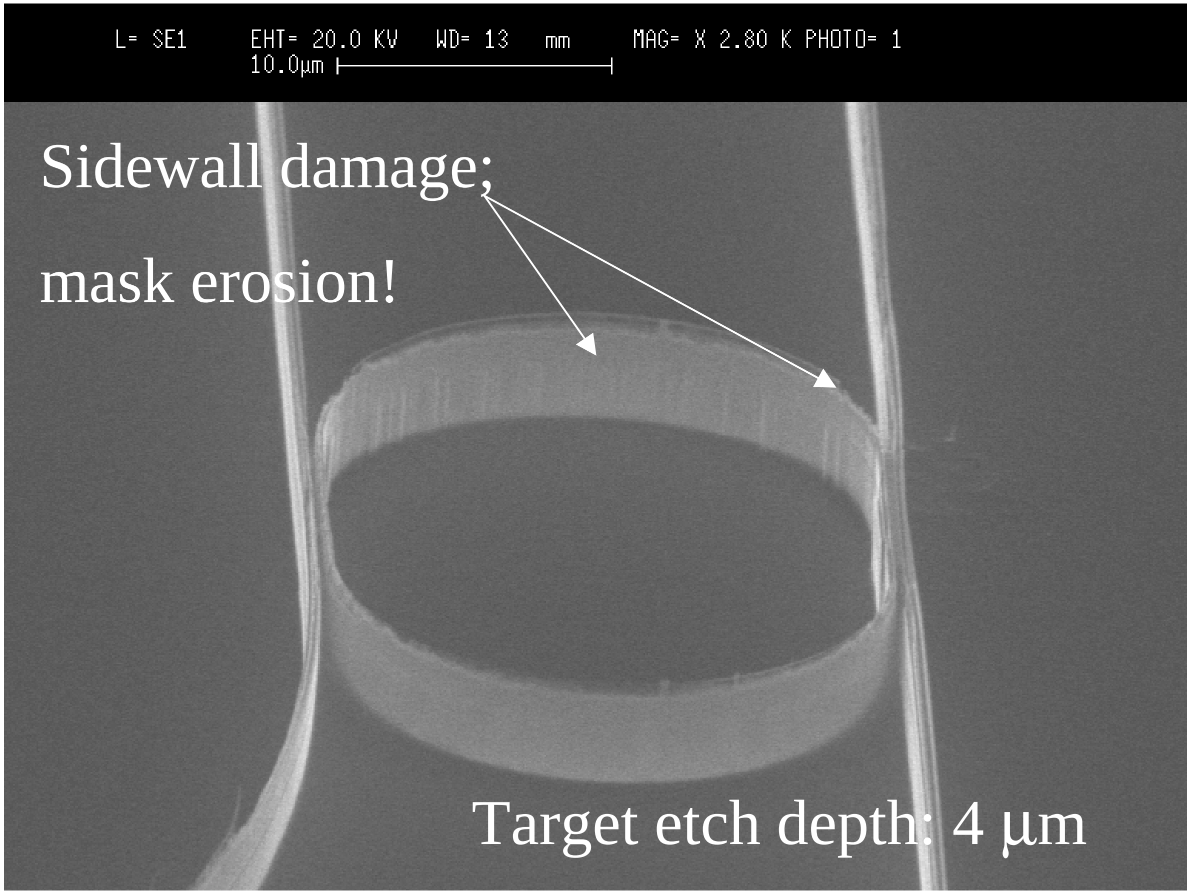
Key Problems with SF_6-patterned Si_3N_4 etch masks:

Mask Erosion Limited Sample Etch Depth to ~3.5 µm :

Insufficient for Isolation! **Rough Sidewalls=> High Loss!**



Key Problems with SF_6-patterned Si_3N_4 etch masks:

Undesirable deposits on the surface of the sample

CONCLUSION: WE MUST USE ANOTHER ETCH MASK!

Choices for Masking Materials

Three broad categories of masking materials:

- Metals: Ni, Cr, NiCr, Ti, Al, W, Pt
- Dielectrics: SiO_x, SiN_x
- Polymers: Photoresist, E-beam resist

METAL MASKS:

- Metal masks are extremely etch resistant and excellent choices for deep etching.
- However, these masks are difficult to remove and the metal grains result in transferred striations.
- Therefore, we opt to NOT use a metal mask for this project

DIELECTRIC MASKS:

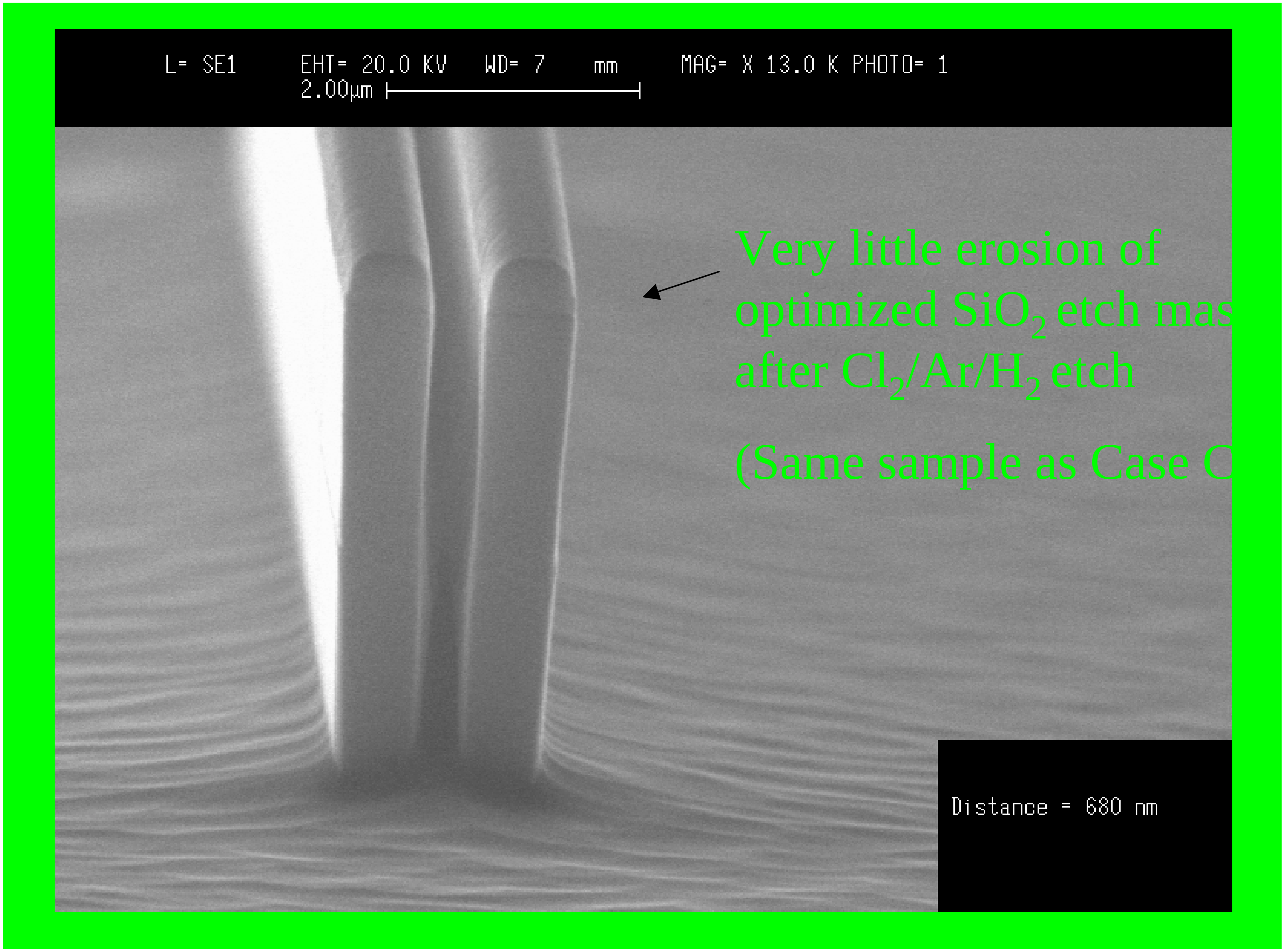
- Dielectric masks have moderate etch resistance, and are often used to etch nanostructures
- Dielectric masks are "soft" and result in very little transferred striations to the underlying material.

POLYMER MASKS:

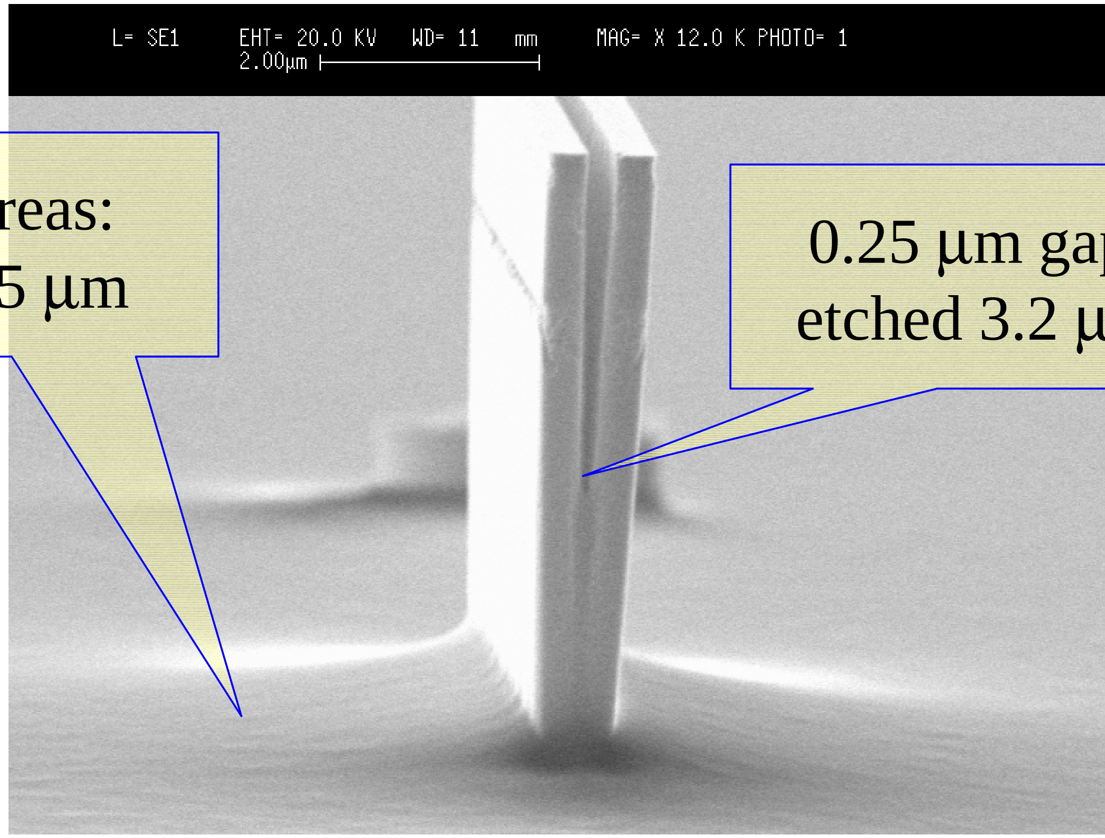
- Fully cured polymers are highly etch resistant, and may be used as masks for deep etching.
- Often have poor etch resistance even when cured
- Certain negative e-beam resists have much better etch stability
- However, by themselves, these resists are not quite sufficient to etch the depths we require.
- Run the risk of chamber contamination

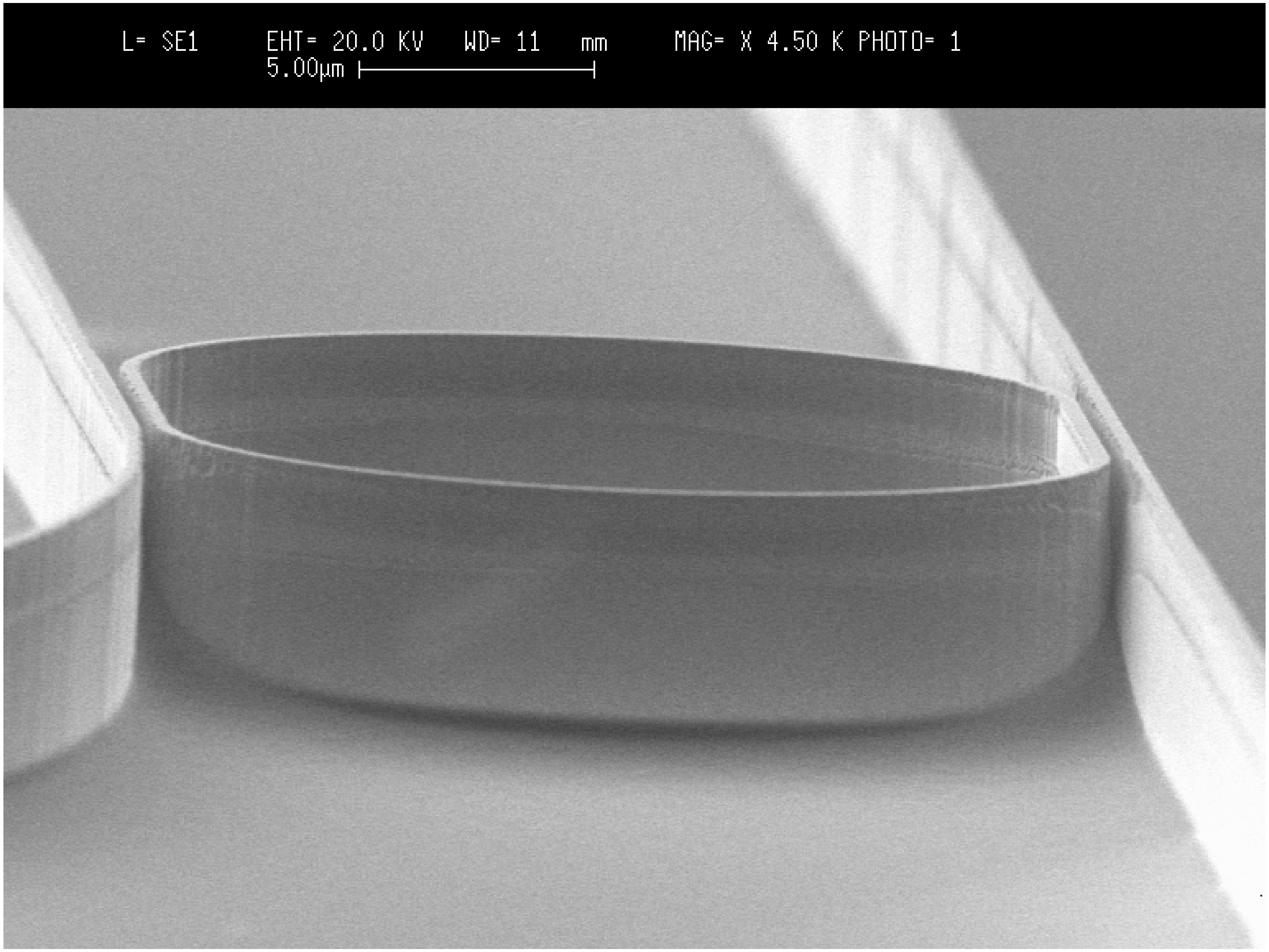
CONCLUSION: SiO_2 is the best choice as an etch mask.

… Profile of the SiO_2 etch mask depends on the process conditions …

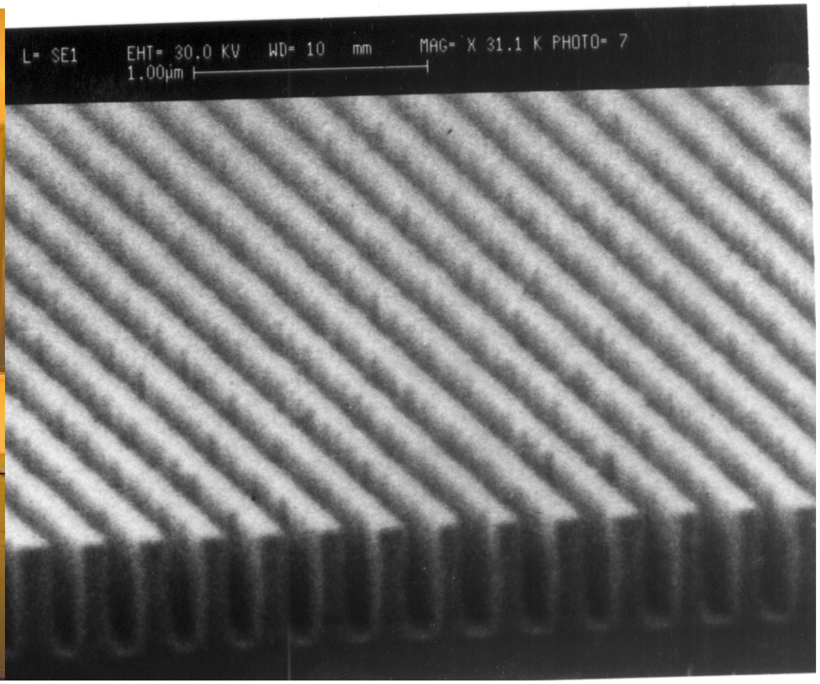

L= SE1 EHT= 20.0 KV WD= 7 mm MAG= X 13.0 K PHOTO= 1
2.00µm
Very little erosion of
optimized SiO_2 etch mas
after $Cl_2/Ar/H_2$ etch
(Same sample as Case C
Distance = 680 nm

Aspect Ratio Dependence of the Etch: Isolation in the Gap




L= SE1 EHT= 20.0 KV WD= 11 mm MAG= X 4.50 K PHOTO= 1
5.00µm

Cambridge EMF 10.5 E-beam Lithography System

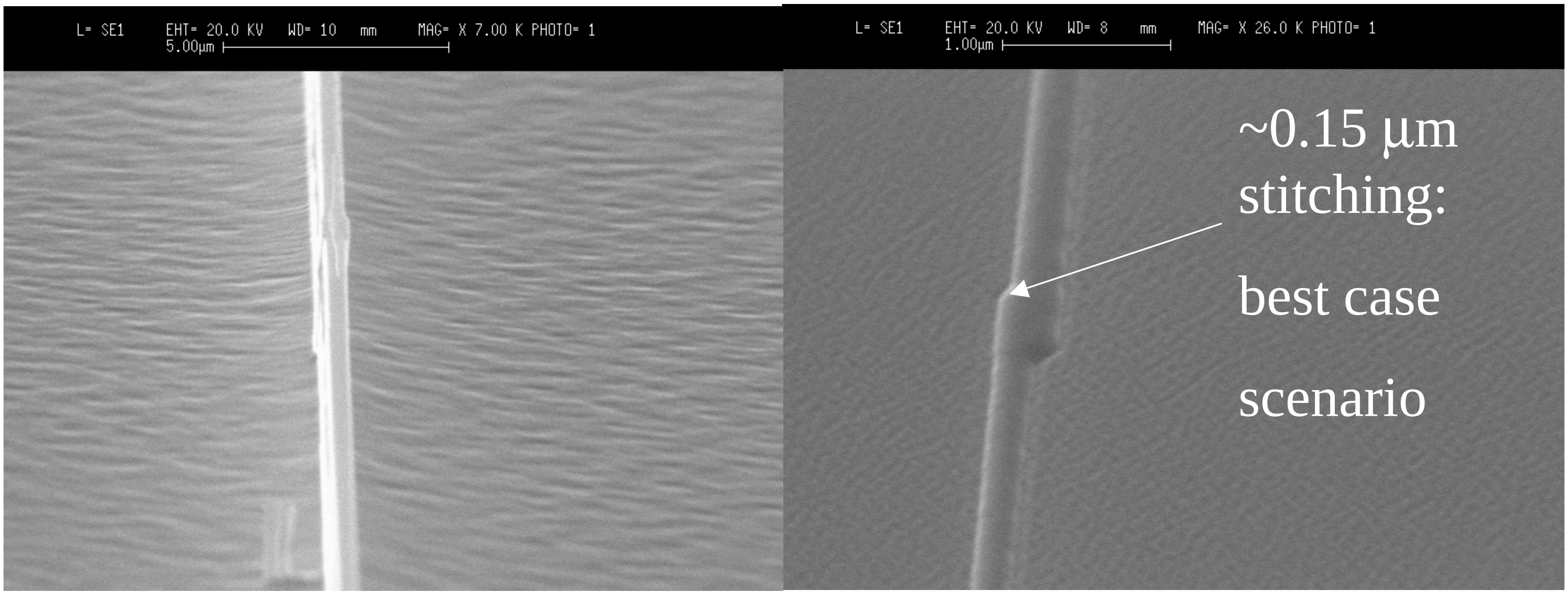


- Linewidth resolution of 100 nm
- 40 kV acceleration voltage
- 0.5- 40 nA beam currents
- Maintained by a full time Research Engineer (staff).

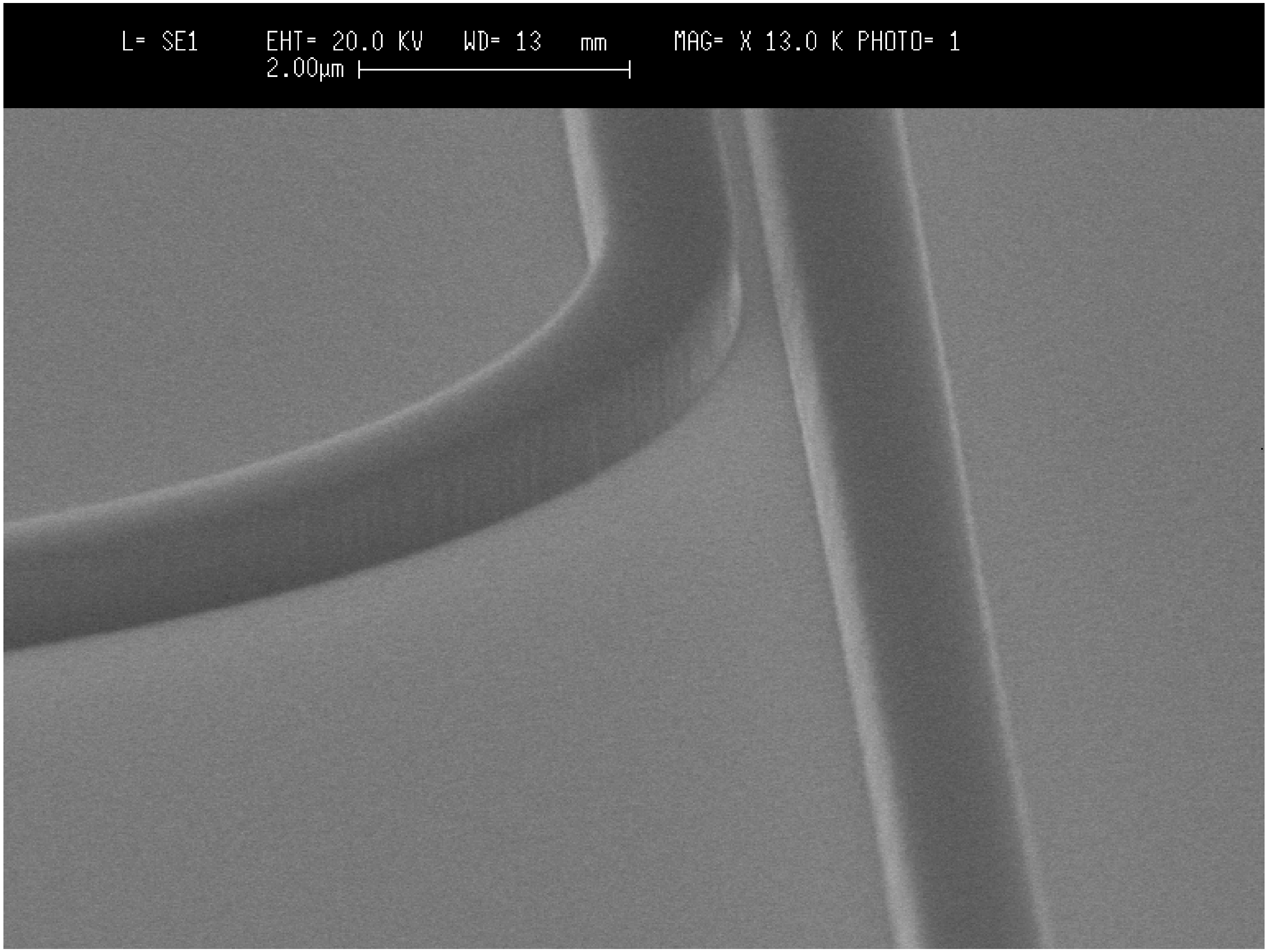
JEOL JBX-6000FS

- Vector Scan, Spot Beam System
- 25 - 50 kV acceleration voltage
- 5 nm minimum beam diameter
- Field Stitching/Overlay accuracy 60/40 nm

Stitching With the Cambridge 10.5 EBMF



Field Stitching With the JEOL 6000 FS:Almost Unnoticeable!



InP-Based Etching for Resonant Enhanced Modulator Development

OBJECTIVES

- Micro-optical Process Development
  - Dry Etching Recipes for InP systems
  - Lithography of dimensions less than 1 μm linewidth with sharp edge acuity
- Device Design and Layout
- Device Processing

APPROACH

- Optimization of the ICP process
- Pattern Definition via E-beam lithography
- Profile Characterization via SEM

ACCOMPLISHMENTS

- Demonstration of highly anisotropic sub-micron features via an optimized $Cl_2/Ar/H_2$ ICP-RIE process
- Development of a robust etch mask, allowing for future investigation of a large parameter space
- Provided Sarnoff with device samples approximately twice a month

PLANS

- Performa study of ICP etch conditions in conjunction with Sarnoff
- Development of alternative ICP chemistries which may minimize waveguide loss.
- Provide Sarnoff with additional samples
- Develop a mask set for full device fabrication in conjunction with Sarnoff

DEVICE FABRICATION TIMELINE:

From date of sample request, assuming normal operating conditions, 2 weeks

1. **PECVD Deposition:** 2 hrs. plus possible chamber cleaning if another material was recently deposited (Max time.

2. **Electron Beam Lithography:** 6 hours for spinning, gun alignment, and exposure. Generally, we coordinate a day when others are writing to save costs. This often adds 3-5 days.

3. **Nitride Pattern Transfer:** Can be accomplished in less than a half hour.

4. **InP/InGaAsP ICP-RIE:** Requires a minimum of 4 hours, including gas purging, chamber clean/seasoning, temperature stabilization, and sample etching.

Note: This schedule also takes into account "typical" maintenance such as filament replacement on the e-beam/ moderate equipment repair. If extensive repairs are required, the schedule would need to be accordingly adjusted.

Technological Status Summary:

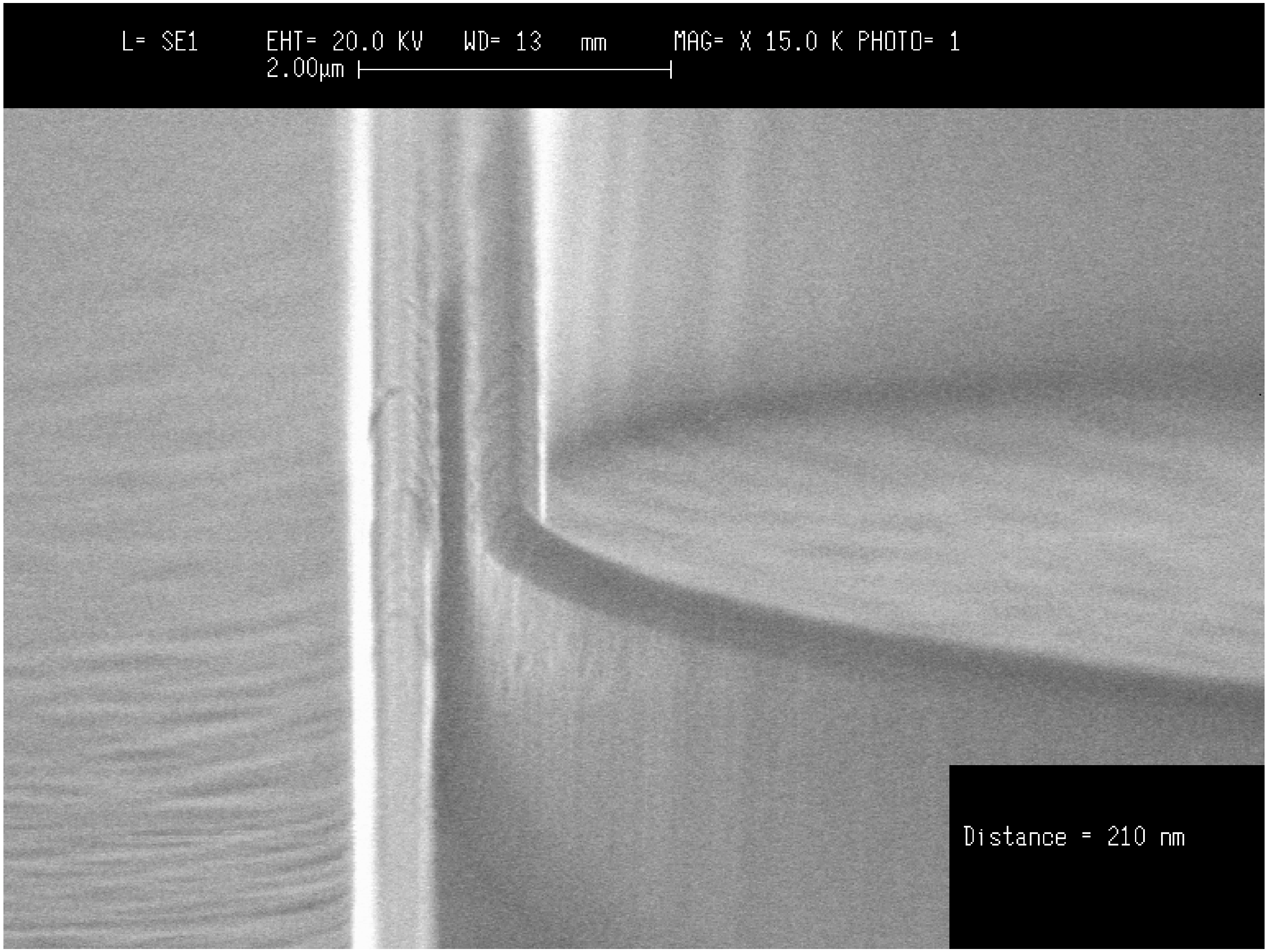
1. **Electron Beam Lithography:** Technique on the Cambridge yields 80% of the patterns (excluding stitching). Preliminary transfer to the JEOL shows improved yield and substantially improved stitching.
2. **Nitride Pattern Transfer:** Process is presently abandoned in favor of an SiO_2 etch mask
3. **SiO_2 Pattern Transfer:** Present RIE process is repeatable; shown to scale with oxide thickness as high as 700 nm.
4. **InP/InGaAsP ICP-RIE:** Present process is repeatable. No adjustments anticipated.

Conclusions

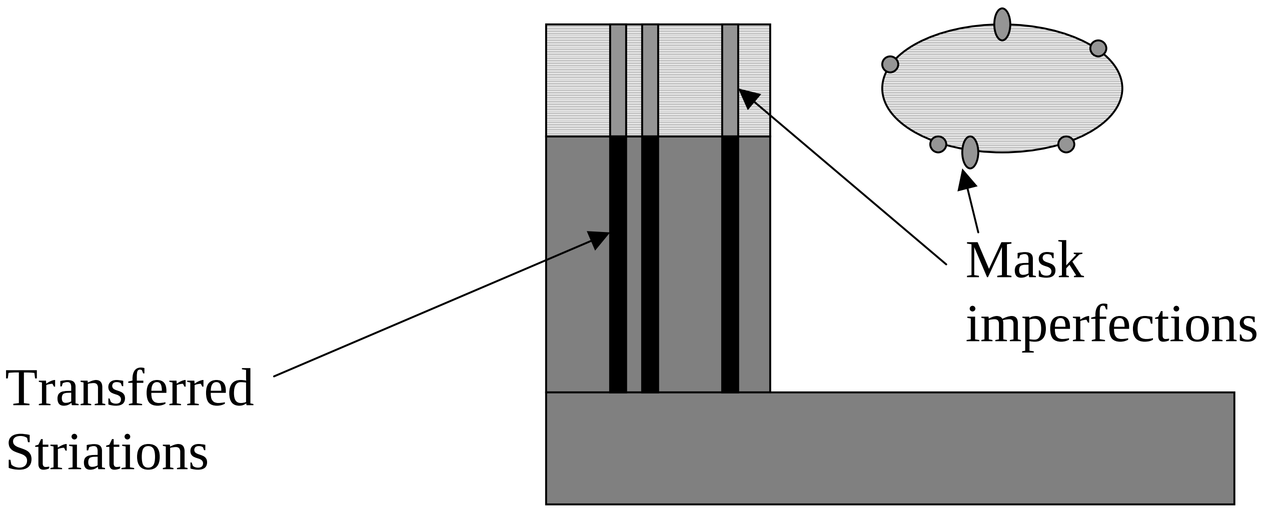
- A $Cl_2/Ar/H_2$ etch chemistry is required to etch anisotropic, submicron features deeper than 2 microns.

- Switching etch mask material from Si_3N_4 to SiO_2 has permitted us to etch substantially deeper without significant mask erosion.

- Improved process control is expected by gradually writing all of the patterns on the new JEOL e-beam. The Cambridge tool will remain as a reserve.

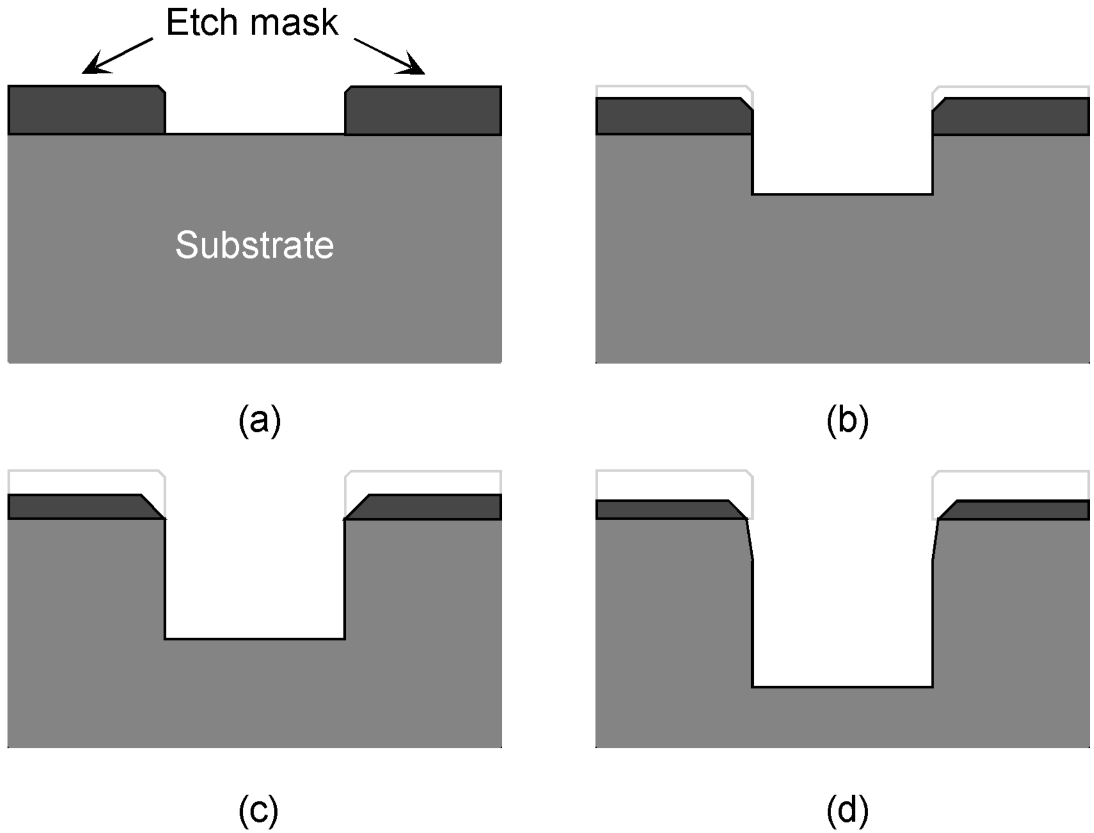

L= SE1 EHT= 20.0 KV WD= 13 mm MAG= X 15.0 K PHOTO= 1
2.00µm
Distance = 210 nm

The "Shower Curtain" Effect



Striations in the sidewall profile are often attributed to existing imperfections in the masking material. The transfer of these striations is known as the "shower curtain" effect.

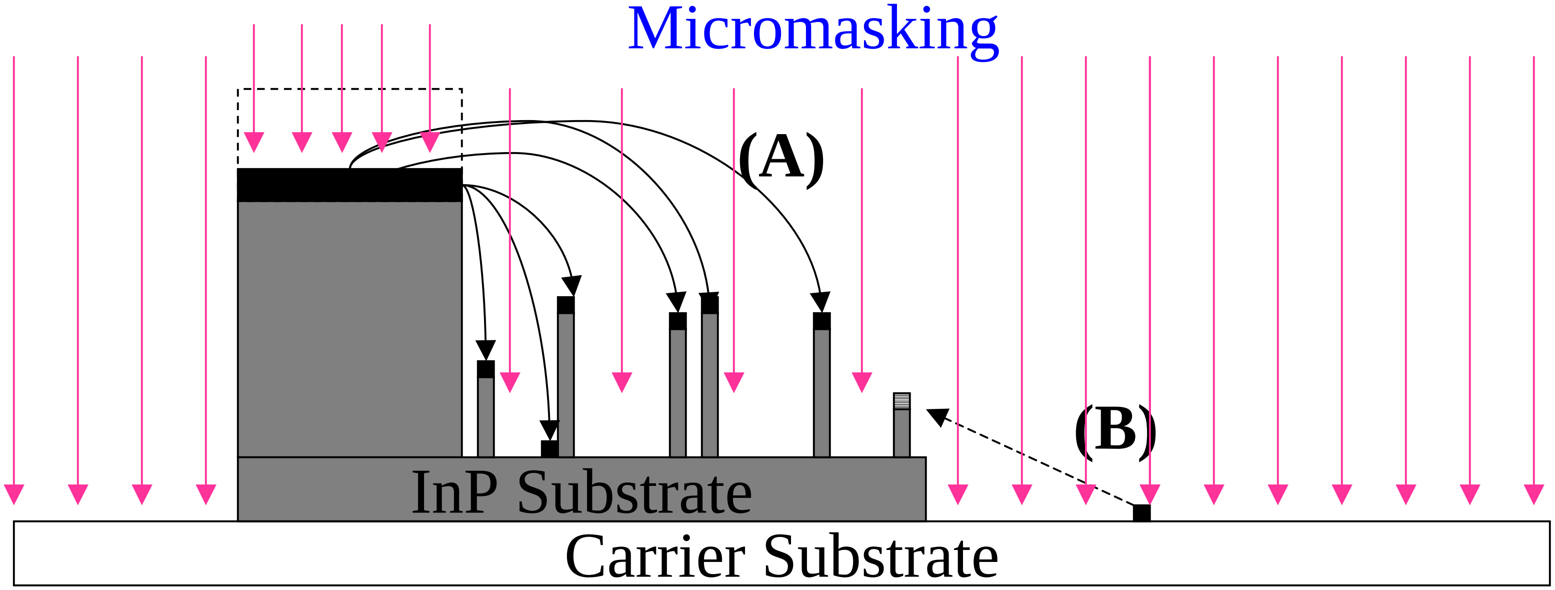
Mask Erosion



To avoid the effects of mask erosion there are two approaches:

- use of an alternate masking material with improved selectivity
- augmenting the thickness of the mask

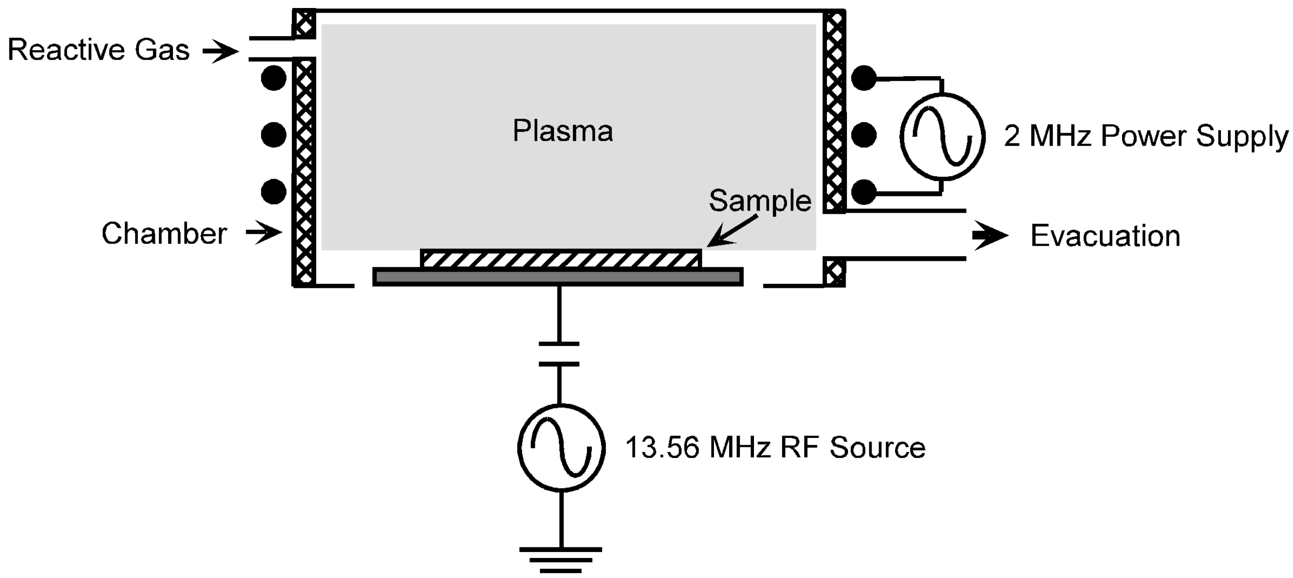
Micromasking



During etching, a phenomenon known as micromasking may lead to the formation of undesirable "grasslike" structures. The source of micromasking is commonly attributed to be:

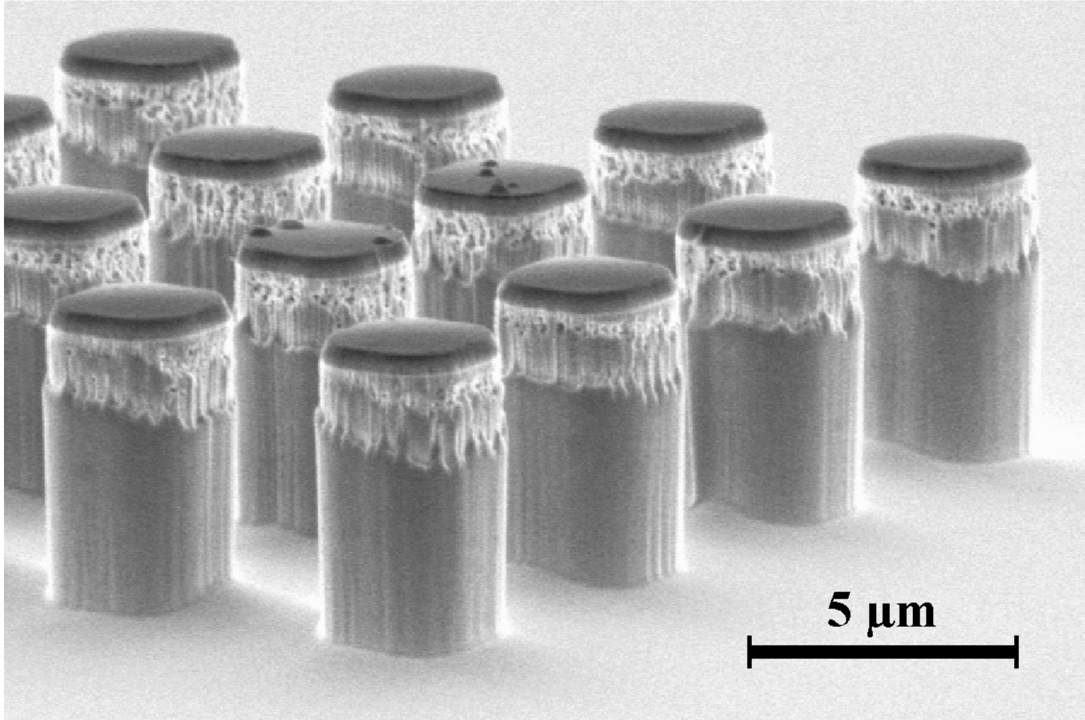
- sputtered etch mask materials (A)
- sputtered material from the carrier substrate (B)

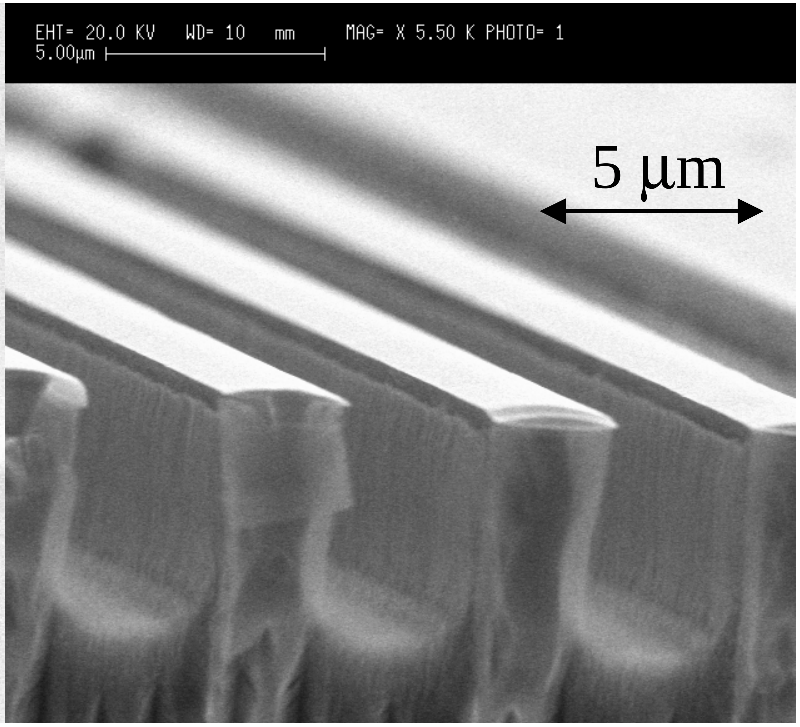
Inductively-Coupled-Plasma Reactive Ion Etching (ICP-RIE)



- RF current supplied through windings around the chamber induce a plasma with a density ($1x10^{11}$-$1x10^{12}$ ions/cm^{-3}) 2-3 orders of magnitude higher than conv. RIE.
- Ion energy may be independently varied by superimposing an RF Bias on substrate.
- Operation at lower pressures than conventional RIE (<10 mT) leads to more directional etching (high anisotropy).
- High ion flux with low energies enables low etch damage while maintaining high etch rates

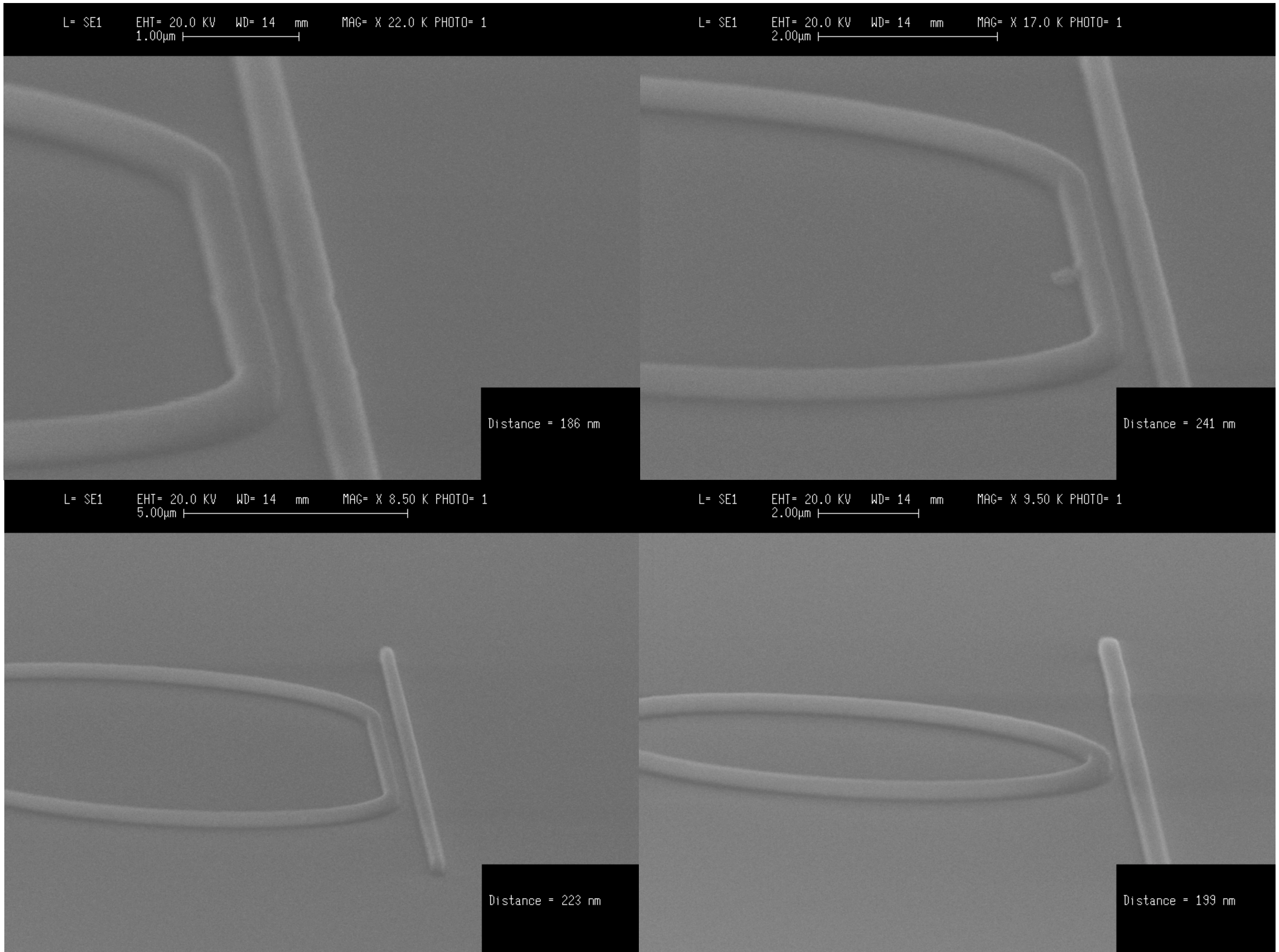
Mask Erosion

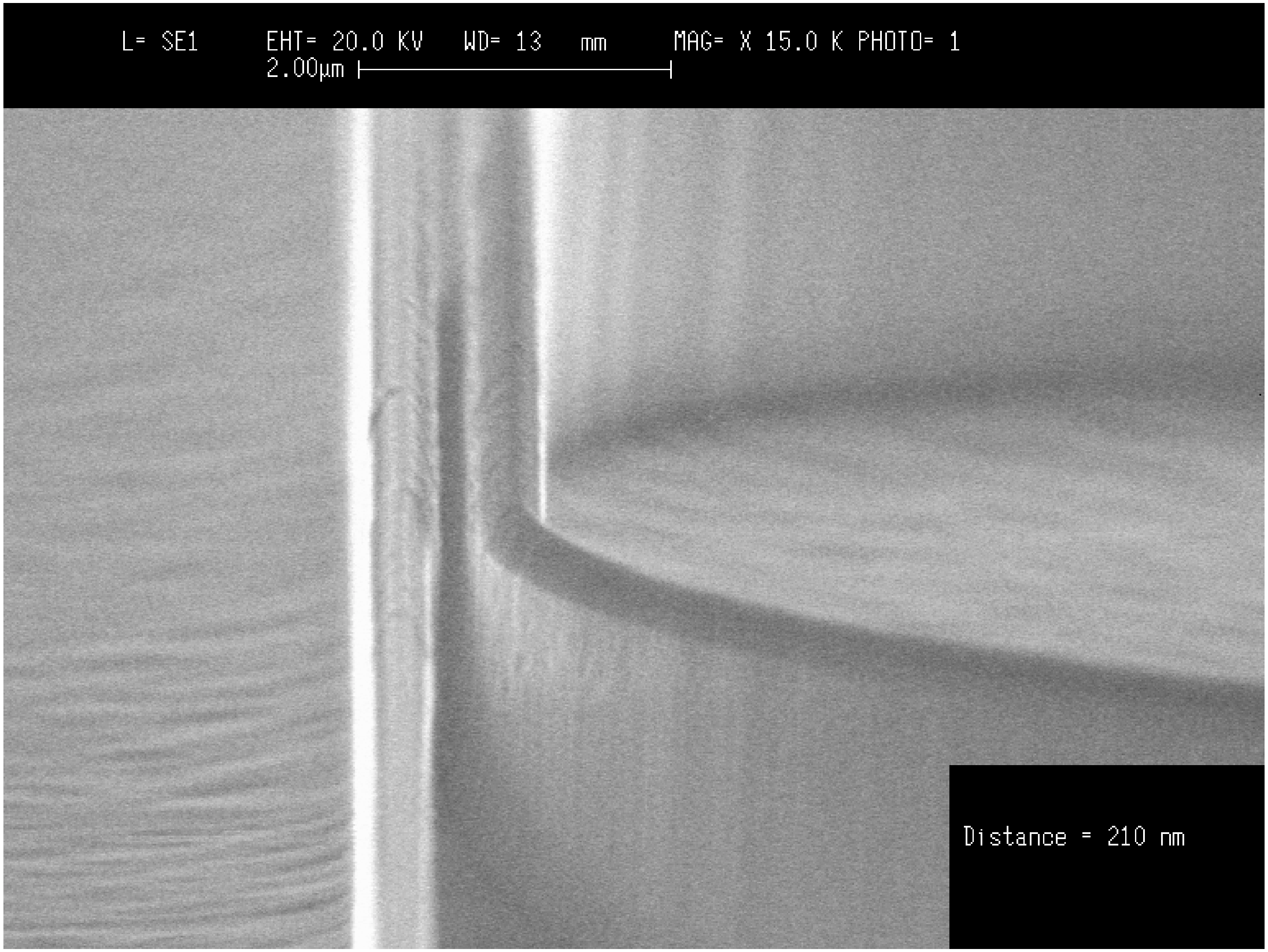




In the above pictures, the mask has begun to deteriorate. Note that while the top of the mesas are rough, the bottom portion remains smooth.

Typical AZPN114 Profiles




L= SE1 EHT= 20.0 KV WD= 13 mm MAG= X 15.0 K PHOTO= 1
2.00µm
Distance = 210 nm